

### ADATE207 Timing Formatter Mixed Signal Formats

By David Oka

The ADATE207 Quad Timing Formatter contains the timing generation, time set memory and the drive and compare logic needed for four digital tester pins (refer to the ADATE207 Data sheet).

The chip architecture is based upon the model of stored waveforms that consist of four events per tester period. The pattern data inputs are addresses into a waveform memory which is used to store the delay and event code for four flexible events per channel. This architecture was inspired by the STIL based waveform definition of patterns but can be used to emulate any digital pin architecture using four or fewer active edges per period. This application note explains how to use the programmable waveform model to emulate the fixed format, fixed pin state use model of conventional digital pins that typically use 6 timing edges per channel.

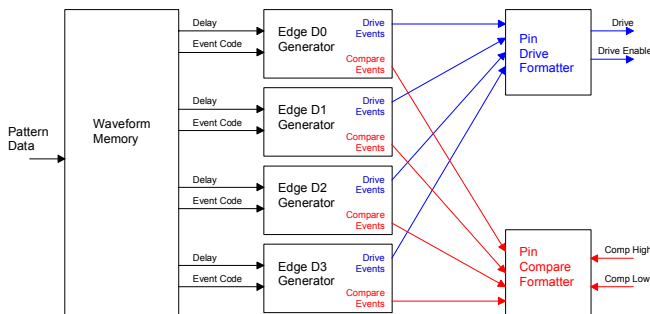


Figure 1 Waveform Based Timing Formatter (one pin of four total)

The ADATE207 waveform based timing formatter block diagram is shown in Figure 1. This block diagram shows one of four channels. It has the following features:

- ♦ 8 Bit pattern data input that addresses up to 256 waveform entries. These 8 bits can be split between time set values and pin states for conventional test systems.
- ♦ 256 deep waveform memory driving 4 event generators per period a maximum period rate of either 100MHz or 200MHz. Each waveform entry consists of a programmed delay value and an event code.
- ♦ Programmed delays for each event can be programmed over a 4 period duration with a maximum delay of 163.8 uS and resolution of 41.7pS.
- ♦ Each event generator can generate one of 6 possible drive events or one of 9 possible compare events which is a superset of the 13 STIL defined events.






- ♦ Pin Drive Formatting logic for driver inputs in normal and in a 2-channel multiplexed mode.
- ♦ Pin Compare formatting logic for failure detection on the dual comparator inputs (Compare High and Compare Low).

### STIL COMPATIBLE EVENTS

The ADATE207 waveform memory contains two fields for each event generator. The delay field consists of a master clock count value and an analog vernier delay value. The event code is a four bit value that specifies either no-action or one of a possible 15 event codes.

The ADATE207 supports a superset of the STIL (IEEE Std 1450-1999) defined waveform events and can be used for a native STIL compatible digital pin.

Each of the four event generators on every tester period can generate either a drive event or a compare event. In the descriptions that follow, D0 – D3 are used to denote events occurring on Drive cycles and C0 – C3 are used to denote events occurring on Compare cycles.

	Identifier	Icon	Definition
N	No Action		No Action or change
0	Drive Low		Drive logic low if the driver is already enabled.
1	Drive High		Drive logic high if the driver is already enabled.
D	ForceDown		Force logic low. Drive to the low voltage level (VIL). If the driver was previously in the off (Z State), then turn the driver on and drive low.
U	ForceUp		Force logic high. Drive to the high voltage level (VIH). If the driver was previously in the off (Z state), then turn the driver on and drive high.
Z	ForceOff		Force logic high impedance. Turn the driver off. Note: The current U/D state is restored if the next drive state is "P"


	Identifier	Icon	Definition
P	ForcePrior		Force logic to last driven state. Turn the driver on and go to the last drive state (i.e., If the last drive state was “D”, then go to low; if the last drive state was “U” then go to high)

Table 1 ADATE207 Drive Events

Any event generator can generate any of the above Drive events, but that is not true for compare events. Window compares use pairs of events and the TGEN does not allow arbitrary pairing of the events. Window compares are designed to use the event pairs of C0/C1 and/or C2/C3. By design, only C0 and C2 events can open windows and only C1 and C3 events can close events.

All events can perform edge compares (L, H, T, V) and compare unknowns (X). The compare unknown events are used for both closing window comparisons and generating edges for DUT Data capturing.

## MIXED SIGNAL FIXED FORMAT PIN STATES

The 256 waveforms can be used to generate the common pin states shown in Table 2. There are 8 bits used as pattern data to address the waveform memory. Given that 3 bits are required to specify the 7 pin states, there are 5 remaining bits that can be used to specify a timing or format set. E.g. These 5 bits can address up to 32 unique timing sets. In this use model, the waveform memory is used as timing set event memory.

Pin State	Encoding	Description
0	0x0	Drive Low
1	0x1	Drive High
L	0x2	Compare Low
H	0x3	Compare High
M	0x4	Compare Mid-Band
X	0x5	Compare Mask
V	0x6	Compare Valid
-	0x7	Repeat (Reserved)

Table 2: Fixed Pin State Pattern Data Encoding

In this perspective the pin could drive any format that can be composed of 4 edges.





	Identifier	Icon	Definition
L	CompareLow	↓	Compare logic low (edge). Compare for a voltage level lower than the voltage threshold (VOL).
H	CompareHigh	↑	Compare logic high (edge). Compare for a voltage level higher than the voltage threshold (VOH).
X x	CompareUnknown		Compare logic unknown. This will not generate a fail regardless of the compare inputs. This event is used to terminate any window compare state. Also may be used to generate a compare edge for DUT data capture.
T	CompareOff	∨ ∧	Compare logic high impedance (edge). Compare for a voltage level between the low threshold (VOL) and the high voltage threshold (VOH).
V	CompareValid	∧ ∨	Compare logic valid level (i.e., not high impedance) (edge). Compare for a voltage level either lower than the low threshold (VOL) or higher than the high voltage threshold (VOH).
l	CompareLowWindow		Compare logic low (window). Terminated by CompareUnknown.
h	CompareHighWindow		Compare logic high (window). Terminated by CompareUnknown.
t	CompareOffWindow		Compare logic high impedance (window). Terminated by CompareUnknown.
v	CompareValidWindow		Compare logic valid level (window). Terminated by CompareUnknown.

Table 3 ADATE207 Compare Events

## QUAD MARKER MODE

In the normal operation of the digital pin, each vector can use up to four events (markers). This is referred to as Quad Marker Mode (QMM), where there is one DUT Vector per tester T0 period input to the TGEN. There are higher speed options trading off events for vectors rate with time sets and markers per vector.

For the 8 bits of pattern data, three bits are used to select one of the 8 possible states listed in Table 2 and five bits are used to specify a time set value. In this mode the upstream pattern generation logic, drives an 8-bit value whose MSB's correspond to 5 bits of time set pointer (i.e. 32 timing sets) and whose LSB's correspond to 3 bits of pattern data.

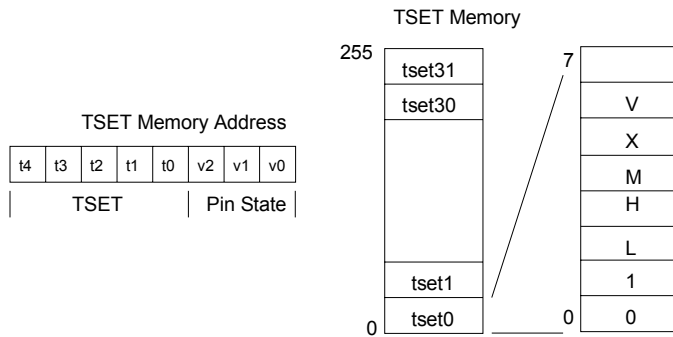


Figure 2 QMM Time Set Memory Address Allocation

Figure 2 shows the time set memory address allocation between the 32 possible timing sets and the 8 possible pin states. The mapping of the pin states to the waveforms are specified via the use of drive and compare formats. There are two drive pin states of 0 and 1. Since each has its own entry in the tset memory, the value of the pin state (0 or 1) is denoted as “Data” in the description of the drive formats.

## QMM DRIVE FORMATS

Drive formats are used to describe a waveform for a given pin state. In general four distinct timing edges (or markers) are needed to produce all of the standard formats. Many formats require only two distinct timing edges and even a single timing edge is sufficient for the common NRZ (Non Return to Zero) format. There is a tradeoff of the number of edges per device vector and the number of time sets available.

During drive pin states the four edges are used to enable the driver, drive up or down (depending upon the drive data), then drive a return level (depending upon the format) and then disabling the driver. The “P” data is present for all “Precede By” and “Surround By” formats, and the “A” data is present for all “Return To” and “Surround By” formats. The hatched rectangle indicates a compare window or edge strobe.

Figure 3. Shows the general four edge drive formats. The D0 edge is used to enable the driver and present the Preceding level to the data value to be driven. The D3 edge is can be used to tri-state the drive on bidirectional pins. Typically only three edges are needed to generate most formats.

The D1 edge is used to drive the data value of the vector. When the vector data represents a drive 1, then the D1 edge is used to drive the 1 value.

The D2 edge is used to change the drive value to the return value.

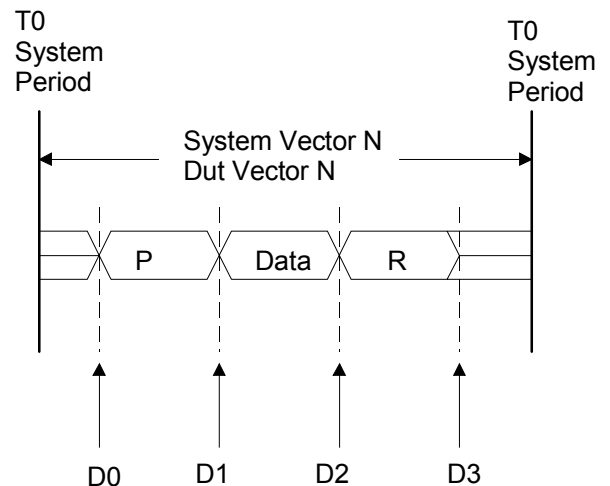


Figure 3. Quad Marker Drive Formats

Table 4 lists an incomplete set of Quad Marker Mode formats. For each format, the action codes for each of the four available edges are shown. The nomenclature of “Data” is used to represent either a code of U or D depending upon the vector data of driving a 1 or a 0 respectively.

Format	Description	D0	D1	D2	D3
NRZ	Non-Return to Zero	P	Data	N	N
NRZT	Non-Return to Zero Tri-State	P	Data	N	Z
NRZC	Non-Return to Zero Complement	P	!Data	N	N
NRZCT	Non-Return to Zero Complement Tri-state	P	!Data	N	Z
RZ	Return to Zero	P	Data	0	N
RZT	Return to Zero Tri-State	P	Data	0	T
RZC	Return to Zero Complement	P	!Data	1	N
RZCT	Return to Zero Complement Tri-State	P	!Data	1	Z
RO	Return to One	P	Data	1	N
ROT	Return to One Tri-State	P	Data	1	Z
ROC	Return to One Complement	P	!Data	0	N
ROCT	Return to One Complement Tri-State	P	!Data	0	Z
RT	Return to Tri-State	P	Data	Z	N

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Format	Description	D0	D1	D2	D3
RTC	Return to Tri-State Complement	P	!Data	Z	N
RC	Return to Complement	P	Data	!Data	N
RCT	Return to Complement Tri-State	P	Data	!Data	Z
RCC	Return to Complement Complement	P	!Data	Data	N
RCCT	Return to Complement Complement Tri-State	P	!Data	Data	Z
MAN	Manchester	P	!Data	Data	N
MANT	Manchester Tri-State	P	!Data	Data	Z
MANC	Manchester Complement	P	Data	!Data	N
MANCT	Manchester Complement Tri-State	P	Data	!Data	Z
CLK	Clock High	P	U	0	N
CLKC	Clock High Complement	P	D	1	N
CCLK	Compare Clock High	P	U	0	N
CCLKC	Compare Clock High Complement	P	D	1	N
HI	Drive High	P	U	N	N
LO	Drive Low	P	D	N	N
OFF	Driver Tri-State	P	Z	N	N
SBC	Surround by Complement	!Data	Data	!Data	N
SBCT	Surround by Complement Tri-State	!Data	Data	!Data	Z
SBCC	Surround by Complement Complement	Data	!Data	Data	N
SBCCT	Surround by Complement Complement Tri-State	Data	!Data	Data	Z
SBO	Surround by One	U	Data	1	N
SBOT	Surround by One Tri-State	U	Data	1	Z
SBOC	Surround by One	D	!Data	D	N

Format	Description	D0	D1	D2	D3
	Complement				
SBOCT	Surround by One Complement Tri-State	D	!Data	D	Z
SBZ	Surround by Zero	D	Data	D	N
SBZT	Surround by Zero Tri-State	D	Data	D	Z
SBZC	Surround by Zero Complement	U	!Data	1	N
SBZCT	Surround by Zero Complement Tri-State	U	!Data	1	Z
SBT	Surround by Tri-State	Z	Data	Z	N
SBTC	Surround by Tri-State Complement	Z	!Data	Z	N
PBC	Precede by Complement	!Data	Data	N	N
PBCT	Precede by Complement Tri-State	!Data	Data	N	Z
PBCC	Precede by Complement Complement	Data	!Data	N	N
PBCCT	Precede by Complement Complement Tri-State	Data	!Data	N	Z
PBO	Precede by One	U	Data	N	N
PBOT	Precede by One Tri-State	U	Data	N	Z
PBOC	Precede by One Complement	D	!Data	N	N
PBOCT	Precede by One Complement Tri-State	D	!Data	N	Z
PBZ	Precede by Zero	D	Data	N	N
PBZT	Precede by Zero Tri-State	D	Data	N	Z
PBZC	Precede by Zero Complement	U	!Data	N	N
PBZCT	Precede by Zero Complement Tri-State	U	!Data	N	Z
PBT	Precede by Tri-State	Z	Data	N	N
PBTC	Precede by Tri-State Complement	Z	!Data	N	N

Table 4 QMM Drive Formats

## QMM COMPARE FORMATS

Compare formats are used to describe a set of events for a vector comparison for a given compare cycle. Compare cycles are those cycles with a pin state of L, H, V, M or X. During these pin states, the driver is disabled and the DUT outputs are checked for the appropriate level. There are two compare formats, a compare window format and a compare strobe format.

Compare windows use a pair of events to describe a window of time within which the DUT outputs should be stable and at the level defined by the compare vector. Figure 4 shows a compare window format. Edge C0 is used to disable the driver if it is driving at the start of the compare cycle. Edges C2 and C3 are used to open and close a timing window respectively. During this window of time, the high and low comparator inputs are assessed for the expected level. A failure is generated if either the expected level is not true at either C2 or C3 edges or if a glitch occurs within the timing window defined by the C2/C3 edge pair. The window open and close events must originate from the same system period, though either event may occur in either that period or the successive period.

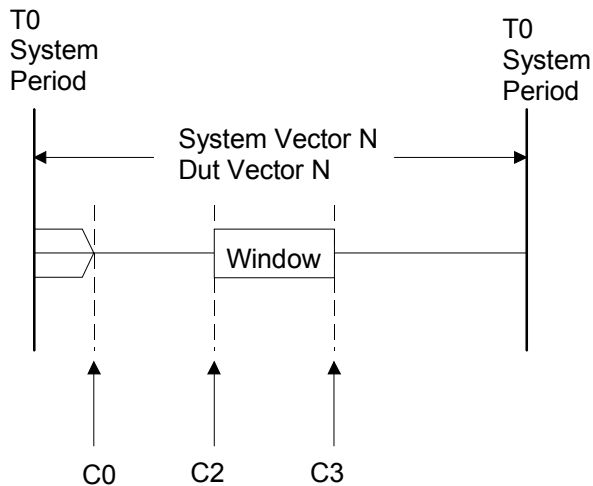


Figure 4 Compare Window Format

Compare strobe format uses a single event to capture the DUT outputs compared against the level defined by the compare vector. Figure 5 shows a compare strobe format.

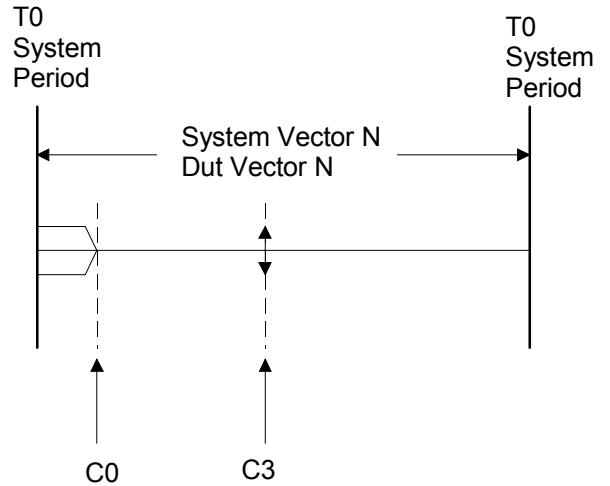


Figure 5 Compare Strobe Format

Compare strobe format uses the D0 edge to disable the driver if it is enabled at the beginning of the period. The D3 edge is used to strobe the high and low comparator inputs and compare the DUT level against the expect vector to generate a failure.

Format	Description	C0	C1	C2	C3
CMPSTB	Compare Strobe	Z	N	N	data
CMPSTBC	Compare Strobe Compliment	Z	N	N	!data
CMPWIN	Compare Window	Z	N	data	x
CMPWINC	Compare Window Compliment	Z	N	!data	x

Table 5 Compare Formats. Data refers to either L, H, T or V for strobe expects and l, h, t, v for window expects of a low, hi, midband or Valid.

Table 5 shows the event setup for compare formats. There are only window or strobe formats available for compare. The strobe format uses C3 for the strobe edge. This presents the fail data in a consistent manner with compare window format with the fail data present on the C3 edge.

## DIGITAL PIN APPLICATIONS SUPPORT

Additional application support for digital pins and the ADATE207 can be found at:

<http://www.loatechnology.com/applications>